A JOURNEY THROUGH UPSTREAM ATOMIC KMS TO ACHIEVE DISPLAYPORT COMPLIANCE

XDC 2017

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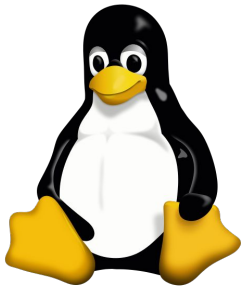
ONLY

Every end user's dream – no black screens

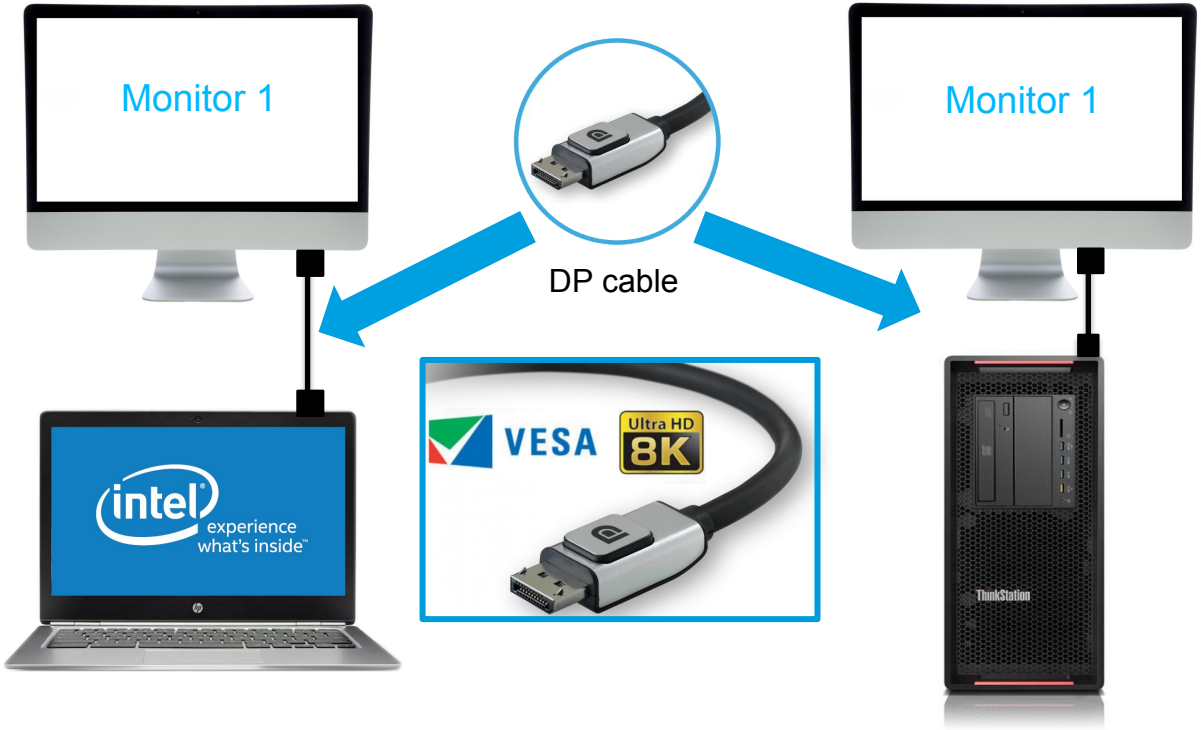
Make Intel graphics kernel driver **DisplayPort*** compliant and **upstream** it



*Other names and brands may be claimed as the property of others.


“A journey of a thousand miles
begins with a single step”

What is DP Compliance?



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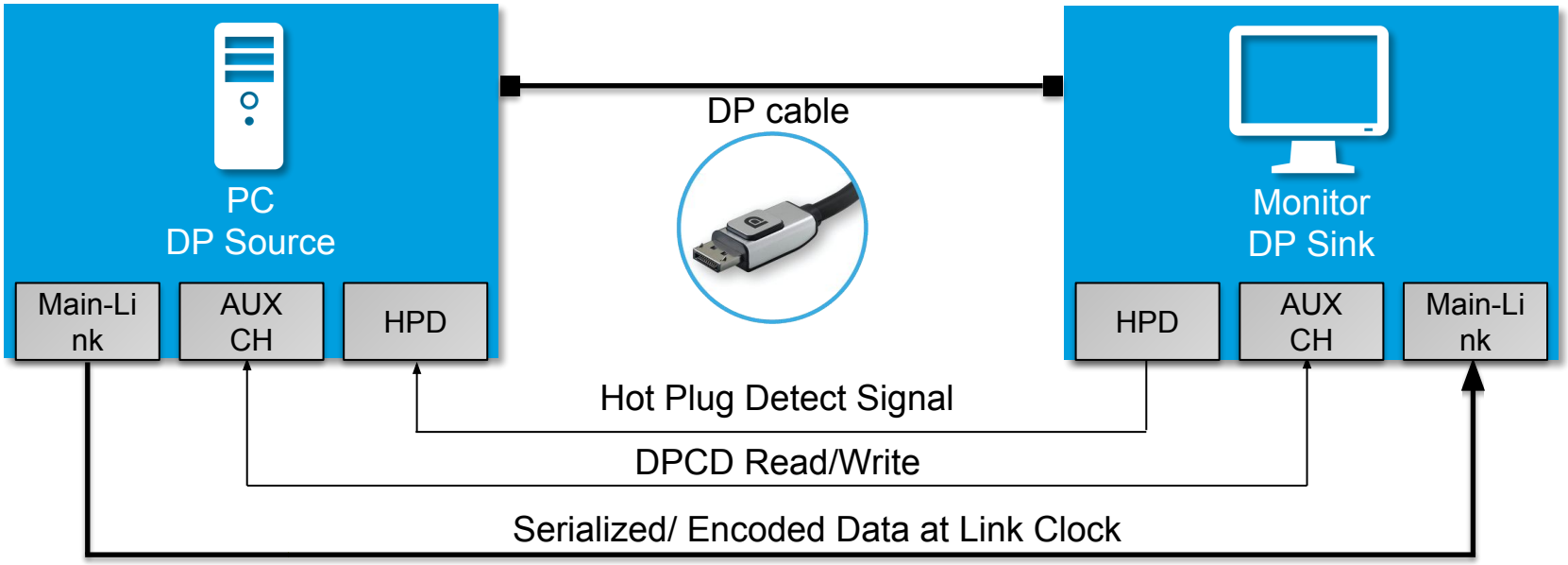
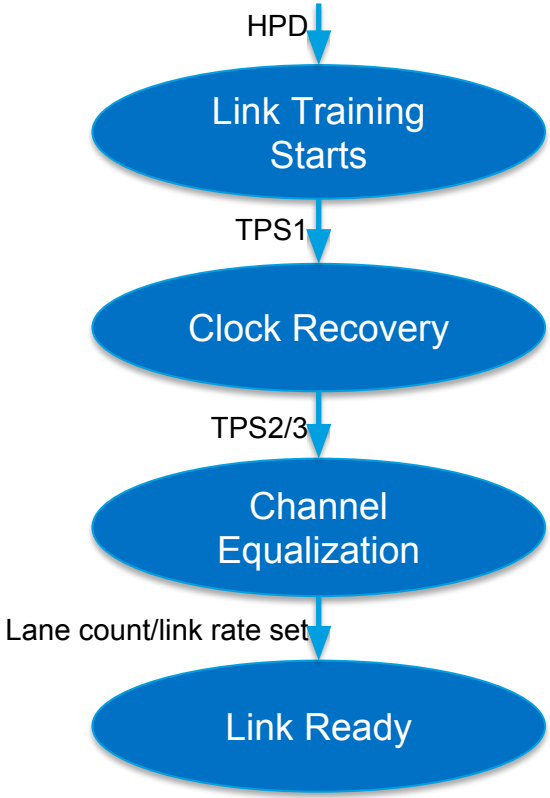
What happens when you connect a DP cable?

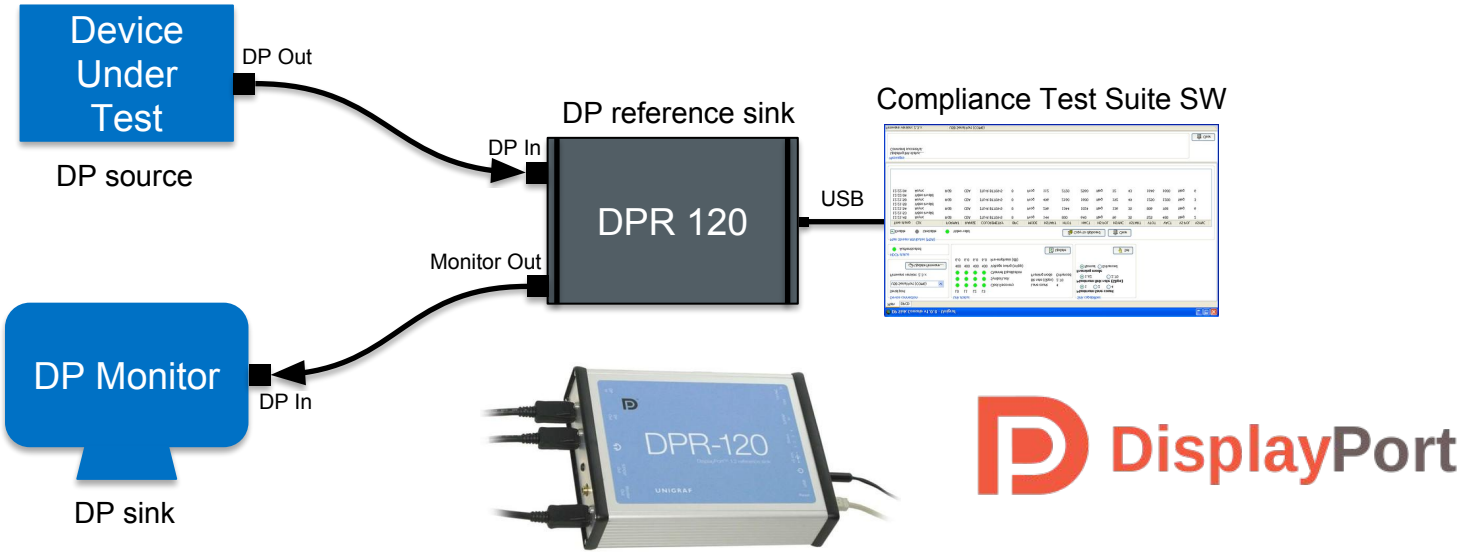


Display Port Link Training

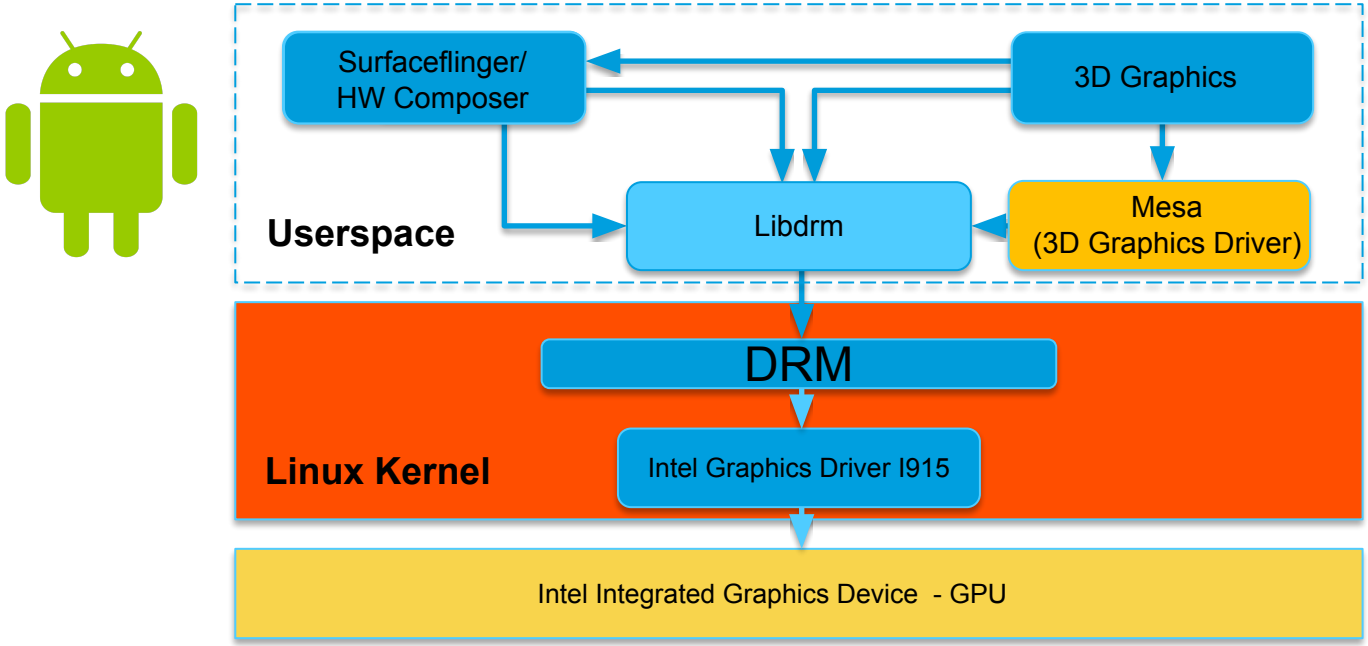
- Main Link Parameters:
  - Lanes – 1, 2 or 4
  - Link Rate – 1.62 , 2.7, 5.4 or 8.1 Gbps/lane
- Link Training:
  - DP source configures the main link through link training sequence



How to test DP compliance?



Who is responsible for DP Compliance?



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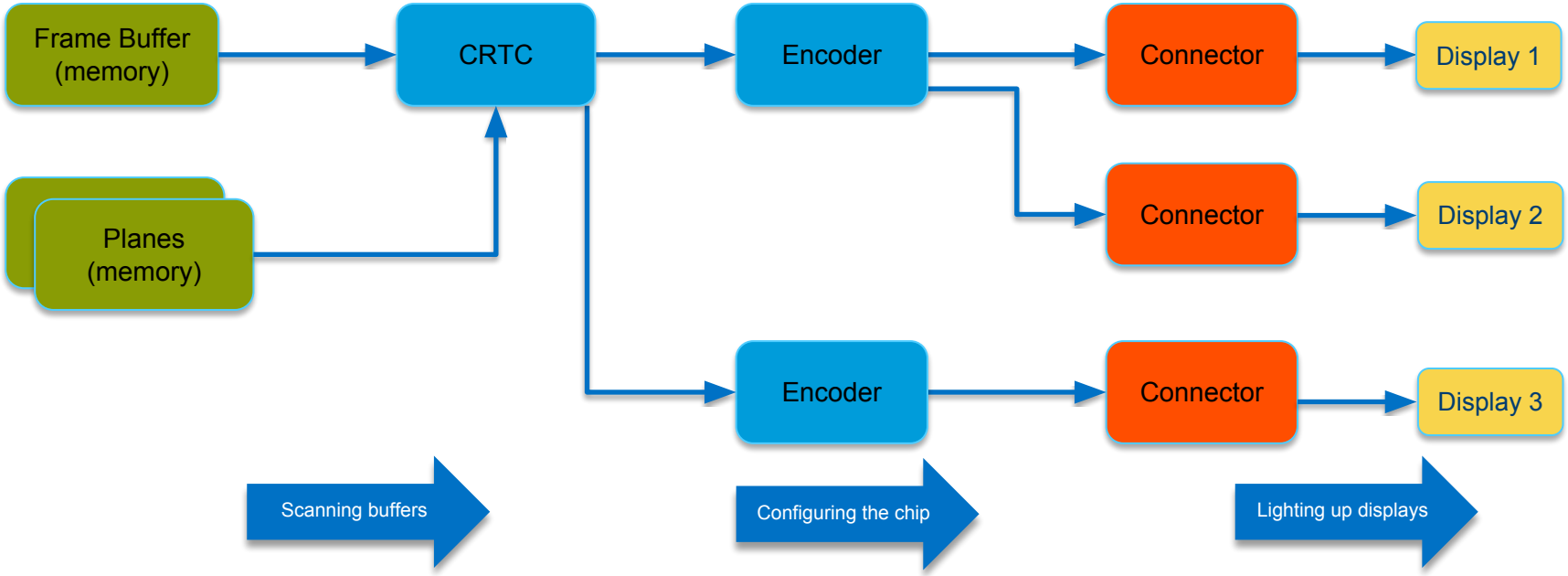
Kernel's Responsibility - Mode setting

Process of setting up clocks, scanout buffers, initializing the chip and lighting up displays



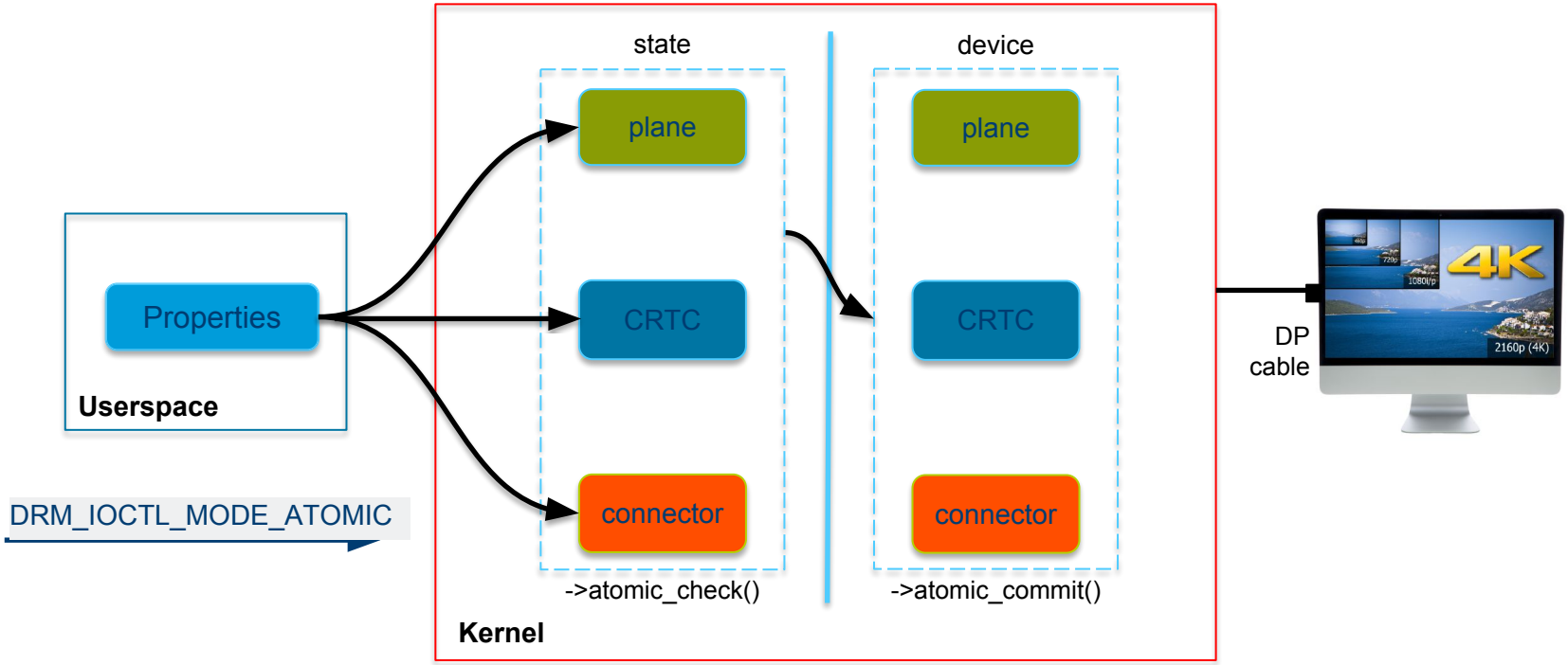
Atomic KMS – Making Kernel and GPU play nicely

An attempt of making “Every Frame Perfect”

An Atomic Operation is the one that appears to take place as a single indivisible operation

Atomic KMS – Making Kernel and GPU play nicely

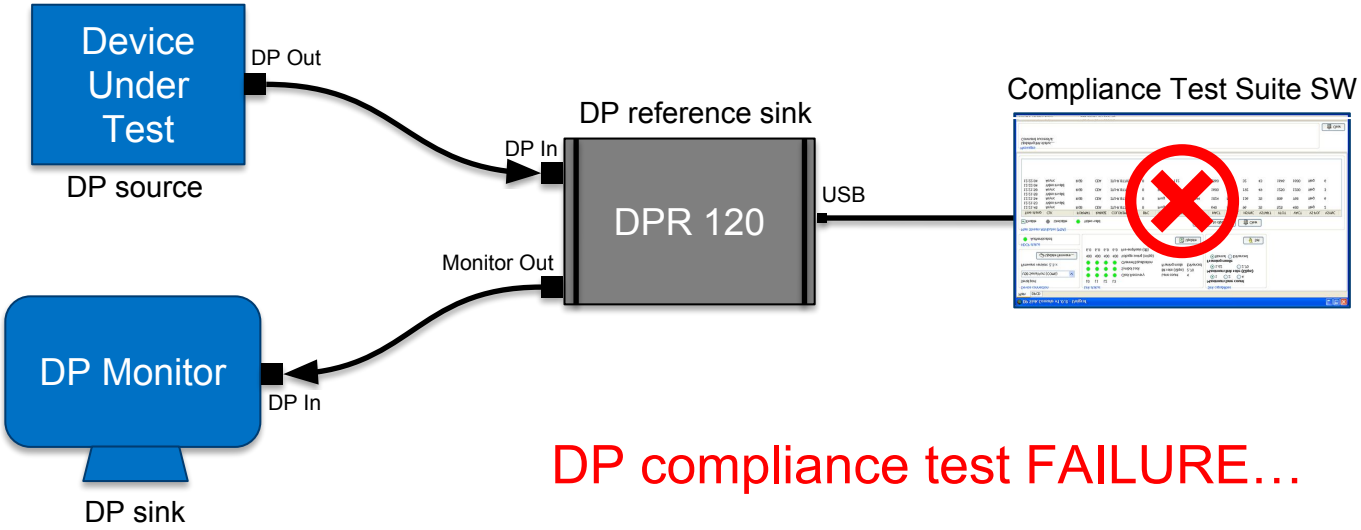
An attempt of making “Every Frame Perfect”



Finally got the ball rolling!!!

Wait, did I
????

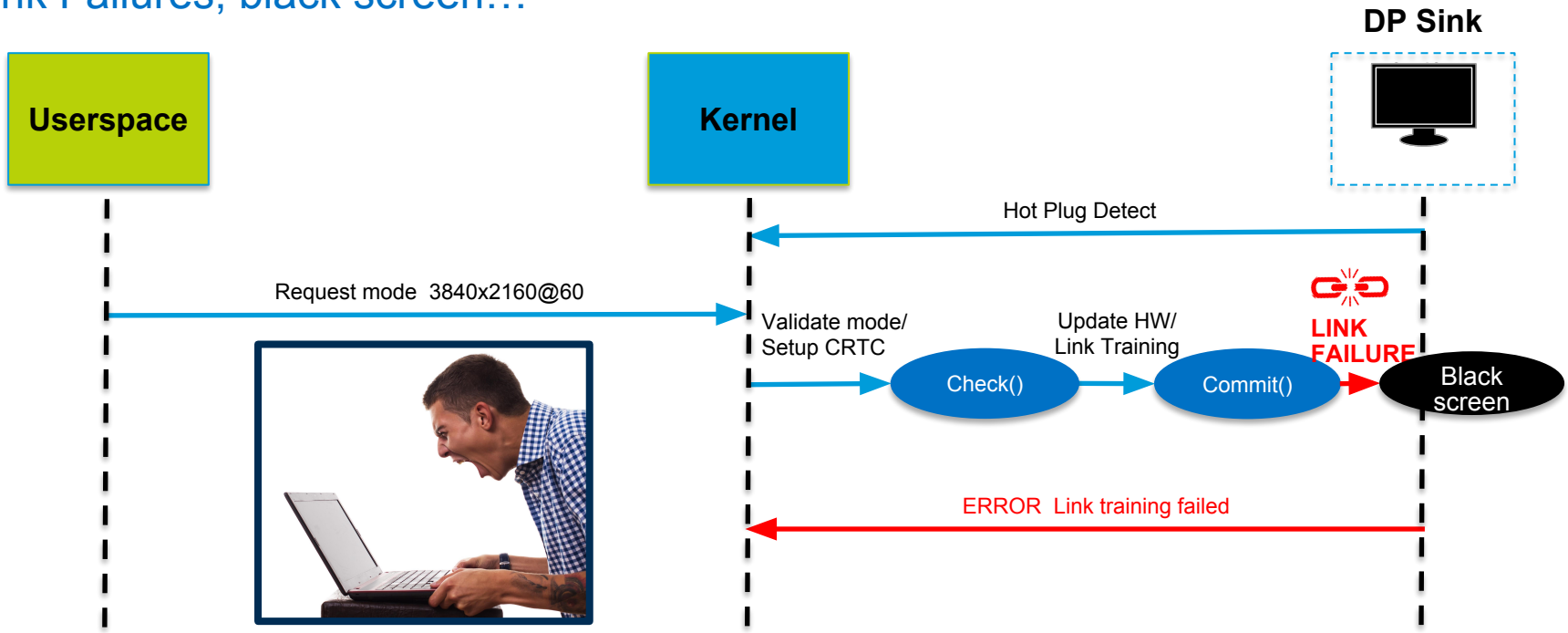
“Anything that can go wrong, will go wrong”



DP compliance test FAILURE…

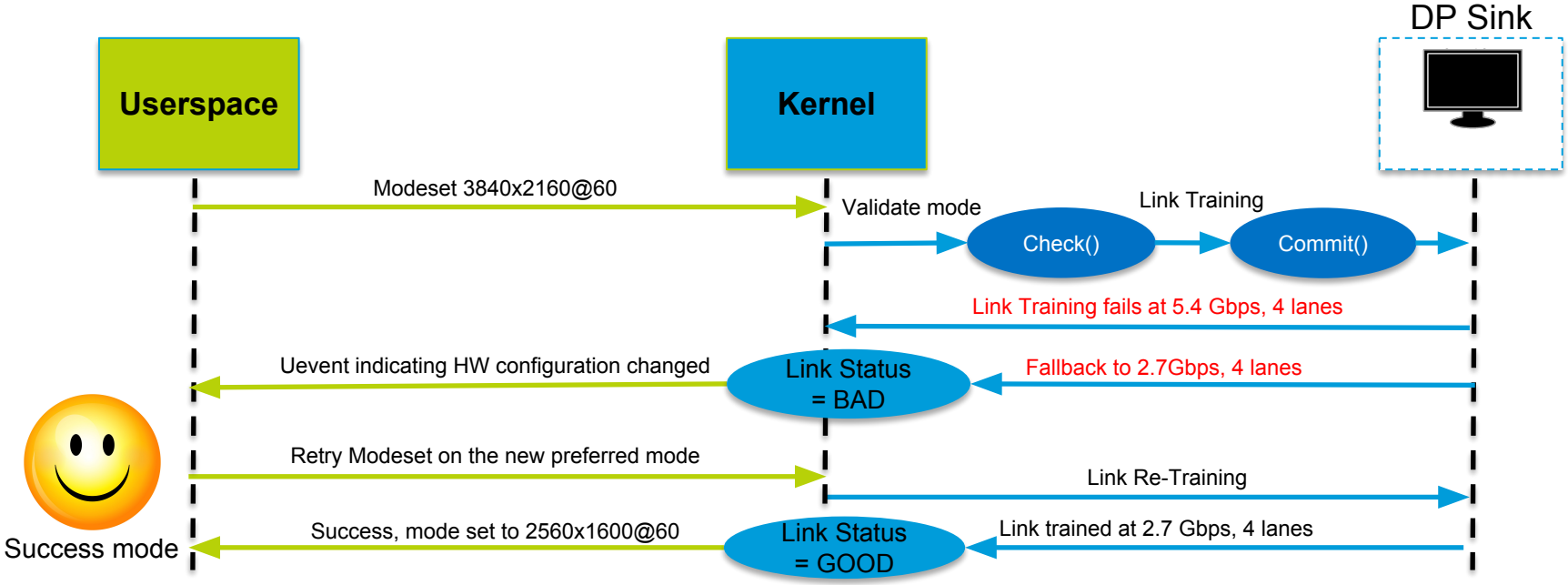
Problem: Does the Atomic KMS driver handle link failures?

Link Failures, black screen…



Solution:

Stable link = Successful Modeset = Perfect frame

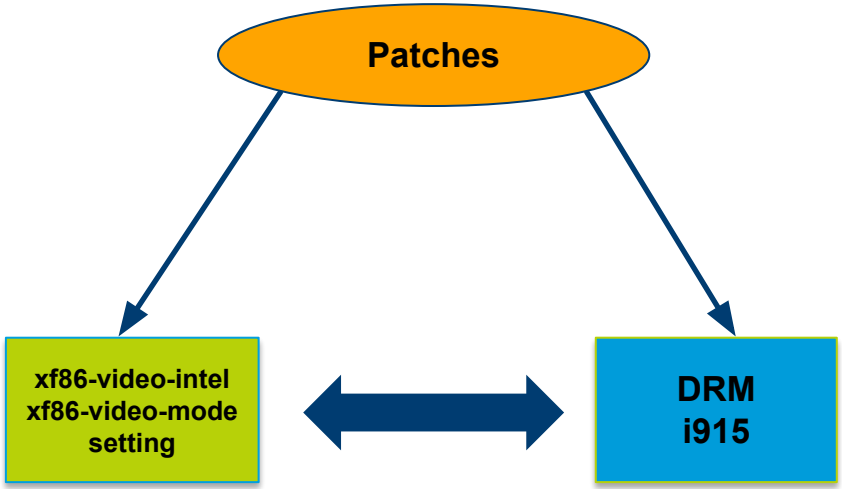


Failure is always an Option….

1. Atomic check guarantees the requested mode
   - Can only check GPU parameters, not the physical DP cable
   - Link training can still fail
2. Link Failure can be asynchronous
   - Link might fail after a successful modeset
3. Atomic allows non blocking commits
   - Return to userspace before modeset has completed

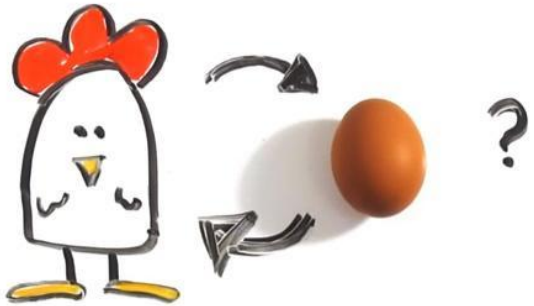
***Asynchronous handling of link failures extremely critical**

Upstreaming Challenge - Coordinating Compliance



Handle
Uevent
Check Link
Status
Retry
Modeset

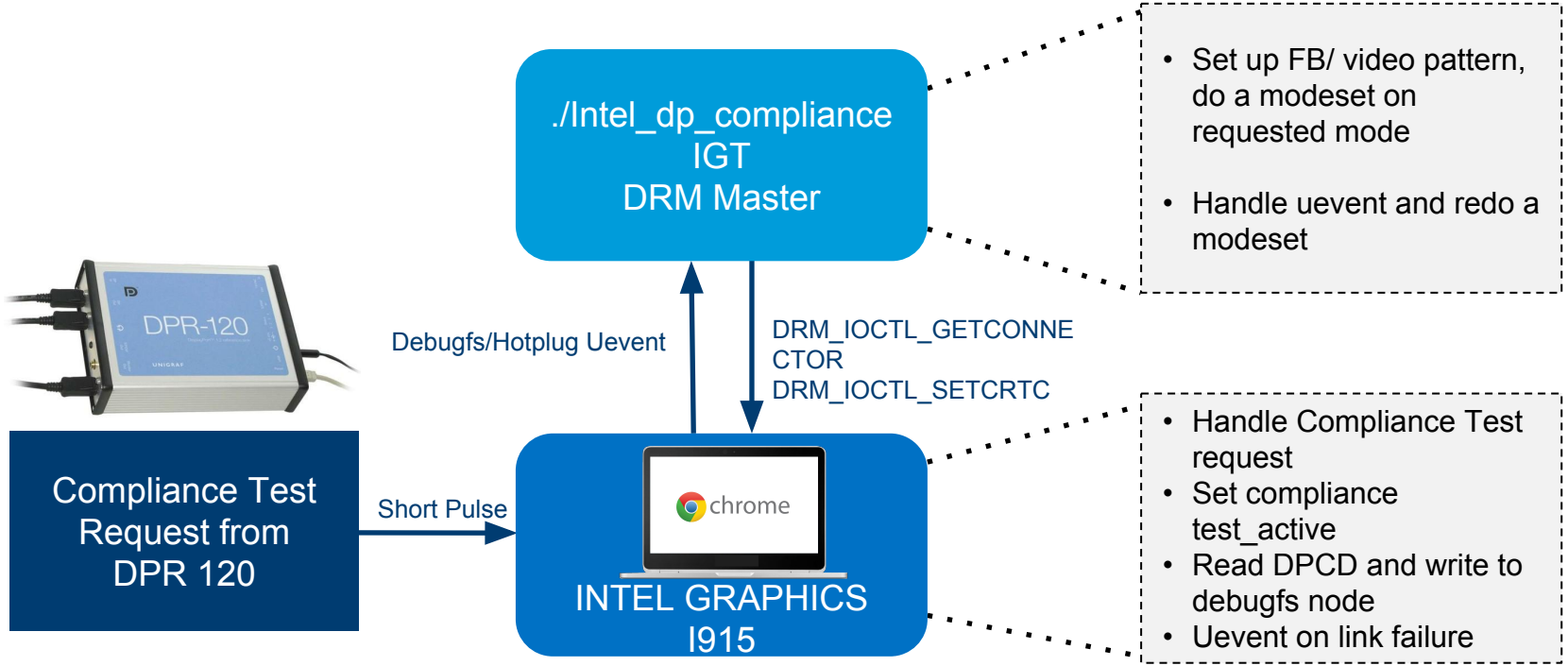
Link Train Fallback
Set Link Status
Send Uevent
Link Retraining



- Old Userspace with new Kernel – Not Compliant
- New Userspace with old Kernel – Not Compliant

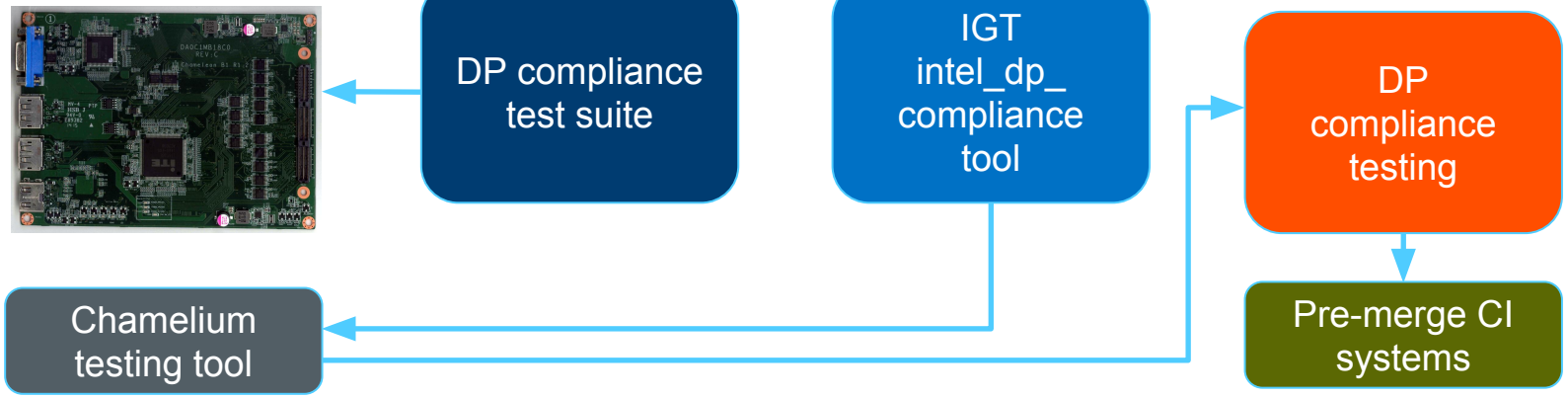
***Both Userspace and Kernel responsible to ensure 100% DP Compliance**

Intel's Responsibility – NO REGRESSIONS



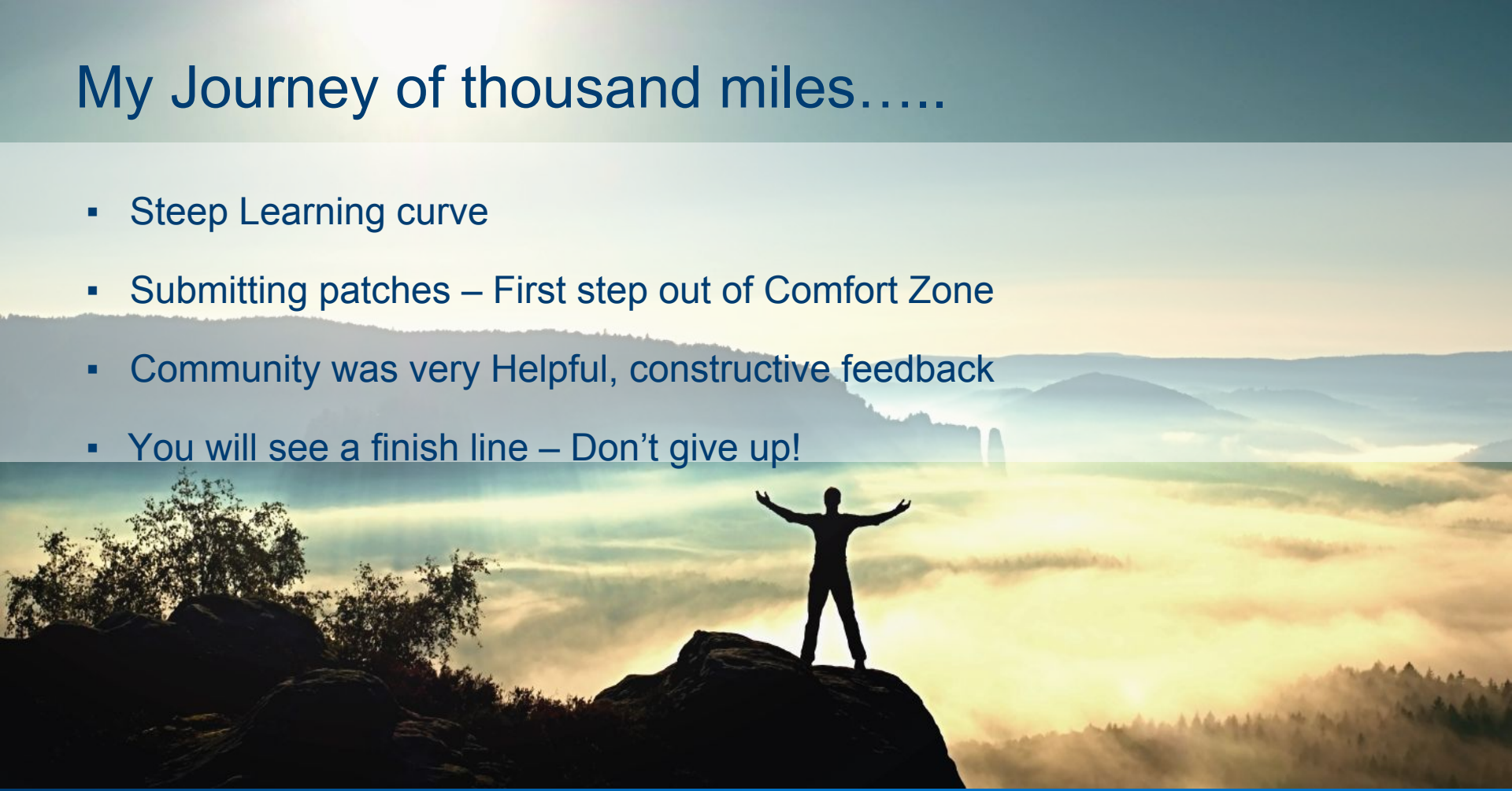
Future steps

- Replace Unigraf's DPR-120 with Google's Chamelium Board
  - ❑ Allows testing all connector types (external displays)
  - ❑ Open Source HW - extend to add all corner cases
- Port the DP compliance test suite (as per VESA CTS) to Chamelium
- Port the IGT intel_dp_compliance tool to Chamelium testing tool.
- Add DP Compliance testing to Pre-merge CI systems



My Journey of thousand miles…..

- Steep Learning curve
- Submitting patches – First step out of Comfort Zone
- Community was very Helpful, constructive feedback
- You will see a finish line – Don’t give up!



Kernel - Daniel Vetter, Jani Nikula, Ville Syrjala, Rodrigo Vivi, Jim Bride, Matt Roper, Harry Wentland, Sean Paul

X - Martin Peres, Chris Wilson, Eric Anholt, Adam Jackson

IGT - Petri Latvala

We are DP Compliant as of
Linux Kernel 4.12 and xorg-server-1.19.3

Questions?

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